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ATOMIC ENERGY OF CANADA LIMITED

L'ÉNERGIE ATOMIQUE DU CANADA LIMITÉE

THE DYNAMIC ANALYSIS FACILITY AT THE CHALK RIVER NUCLEAR LABORATORIES

Installation d'analyse dynamique à Chalk River

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Chalk River, Ontario

October 1979 octobre

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Résumé

L'installation d'analyse dynamique de Laboratoires nucléaires de Chalk River de L'Energie Atomique du Canada, Limitée est un ordinateur hybride comprenant deux calculateurs analogiques AD/FIVE de Applied Dynamic International, un calculateur numérique PDP-11/55 de Digital Equipment Corporation (DEC) et un système de réalisation de programme fondé sur un calculateur numérique DEC PDP-11/45.

Ce rapport décrit les fonctions des divers matériels composant l'installation d'analyse dynamique ainsi que leurs interactions.

On y trouve également une brève description des programmes mis à la disposition des utilisateurs.

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ABSTRACT

The Dynamic Analysis Facility at the Chalk River Nuclear Laboratories (CRNL) of Atomic Energy of Canada Limited (AECL) comprises a Hybrid Computer, consisting of two Applied Dynamic International AD/FIVE analog computers and a Digital Equipment Corporation (DEC) PDP-11/55 digital computer, and a Program Development System based on a DEC PDP-11/45 digital computer.

This report describes the functions of the various hardware components of the Dynamic Analysis Facility and the interactions between them.

A brief description of the software available to the user is also given.

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1. INTRODUCTION

The Reactor Control Branch at the Chalk River Nuclear Laboratories (CRNL) is engaged in the development of dynamic analyses and design and control techniques required for the definition of control and safety system strategies for advanced CANDU power plants and related nuclear systems. To perform this task, computer facilities are required on which to develop detailed dynamic models. Some of the desirable features of such facilities are [1]:

- real-time simulation, implying high speed of computation
- good man/machine interaction, i.e. rapid solution turnaround
- ability to accept process hardware, e.g. a process-control computer
- ease of programming
- good computational accuracy.

A real-time simulation is one in which the various models duplicate the dynamic events that occur in the real system, on the same time scale. Thus, real-time simulation gives the analyst a "feel" for the dynamics of the system being studied. Analog computers are well-suited for this type of simulation because they can solve coupled, mathematical equations in parallel, and continuously in time, whereas digital computers perform mathematical operations serially, in discrete time steps.

The analyst must be able to repeat solutions rapidly, to explore efficiently the effect of parameter changes while developing and learning to control a model. This is defined as good man/machine interaction and is also easy to achieve on an analog computer.

For some simulations, it is desirable to connect certain reactor and process instrumentation directly to the models. A typical example is a process-control computer connected to a detailed CANDU power plant simulation. Here real-time simulation is mandatory since, to develop realistic control algorithms, the model representing the plant must be operating in real time.

It is well known that digital computers are inherently more accurate than analog computers. However, since the accuracy of any simulation is determined largely by the accuracy of the input data, i.e. the physics and engineering parameters, and to a lesser degree by the method of computation, the analog computer is quite adequate for dynamics simulation and control studies.

The digital computer is superior to the analog computer in the handling of large amounts of data, or function arrays, and the implementation of complex logic decisions. On the other hand, high-speed, parallel computation is best done by analog computers. Therefore, the logical choice for large-scale dynamic simulation is a facility which combines the best features of both computer types, i.e. the hybrid computer.

As a result of the arguments presented above, a large, modern hybrid computer system was purchased by the Reactor Control Branch in 1975 March. This system, called the Dynamic Analysis Facility, consisted of two Applied Dynamics International (ADI) AD/FIVE analog computers, and a Digital Equipment Corporation (DEC) PDP-11/45 digital computer.

In 1978 April, a DEC PDP-11/55 digital computer was added to the system, which was subsequently reconfigured into

- a Hybrid Computer, comprising the PDP-11/55 digital and the two AD/FIVE analog computers, plus peripherals, and
- a Program Development System, based on the PDP-11/45 digital computer.

In this report, we describe the functions of the various hardware components of the present Dynamic Analysis Facility, shown schematically in Figure 1, and the interactions between them. A brief description of the software available to the user is also given.

2. ANALOG COMPUTER HARDWARE

The objective of simulation is the solution of man's mathematical approximation of nature, namely differential equations, in the most efficient and accurate way possible. Analog computers are very flexible tools for the solution of sets of differential equations because they offer true parellel processing which can yield many solutions per second.

The high computational speed and flexibility of the analog computer permits many dynamic processes and systems to be simulated in real time, faster than real time, or slower than real time, as appropriate. This property of the analog computer leads to excellent man-machine interaction whereby an analyst can develop a "feel" for his problem, which often results in a more rapid solution, or optimization, of a problem.

Because the analog computer uses voltages to represent problem variables, it is relatively easy to add standard process-control hardware to a simulation. Also, the simulation of a small part of a process system may be connected directly to the actual system for evaluation of its behaviour.

Modern analog computers contain, in addition to the standard analog computing modules, a selection of digital logic elements such as gates, flip-flops and counters. These logic elements are invaluable for the control of problem solutions since the logic states may be controlled by

- the magnitude and sign of problem variables,

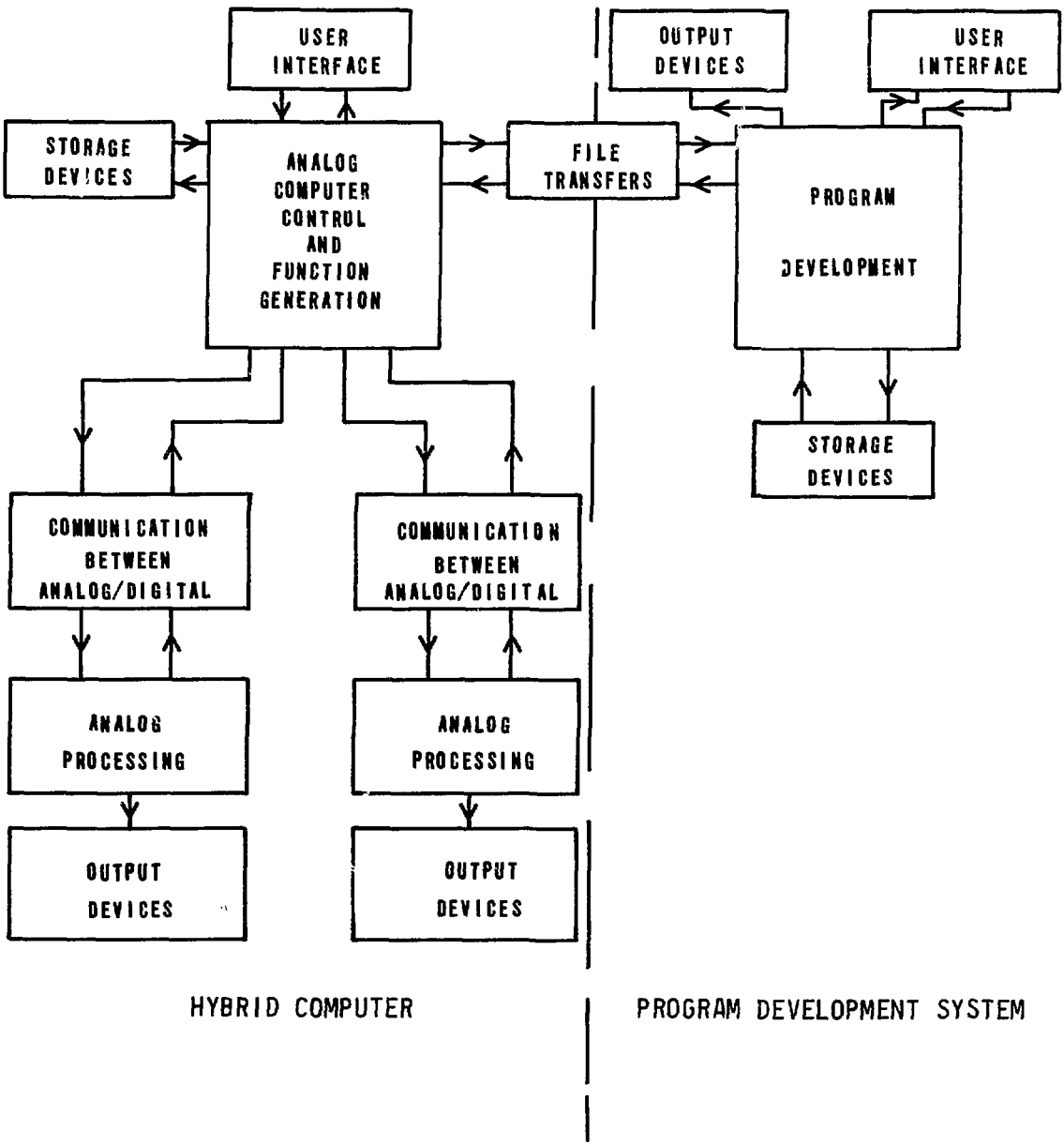

FIGURE 1 FUNCTIONAL DIAGRAM OF THE DYNAMIC ANALYSIS FACILITY

- signals from the analog-computer control system, and
- accurate timing pulses contained in the analog computer.

In a hybrid configuration, the digital computer can also control the execution of the logic program.

As stated above, the analog portion of the Dynamic Analysis Facility consists of two Applied Dynamics AD/FIVE analog computers [2]. These are general-purpose machines, which may be used to solve any problem that lends itself to solution on an analog computer. The reference voltage of the AD/FIVE computer is ± 10 volts.

Apart from their hybrid mode of operation, the two analog consoles may be used independently as stand-alone analog computers. They may also be connected together to form one large analog computer, via a master-slave relationship.

For inter-console communication, there are 110 analog signal trunks, 55 of which are addressable, and 20 logic trunks. However, 10 logic trunks become dedicated when the machines are slaved.

2.1 The AD/FIVE Mainframe

An AD/FIVE console is shown in Figure 2. The operator control panel, logic control panel with indicators, digital access panel and analog-overload indicator panel comprise the left quarter of the machine. The patchboard and computing elements occupy the centre, while 120 digital coefficient units are in the right cabinet.

The patchboard is divided vertically into two fields, each field having an upper logic section and upper and lower analog sections. Each field has six areas which extend horizontally for six patchboard holes per area, and vertically through all three sections (logic and upper and lower analog). Each area has components clearly labelled and numbered (see Figure 3).

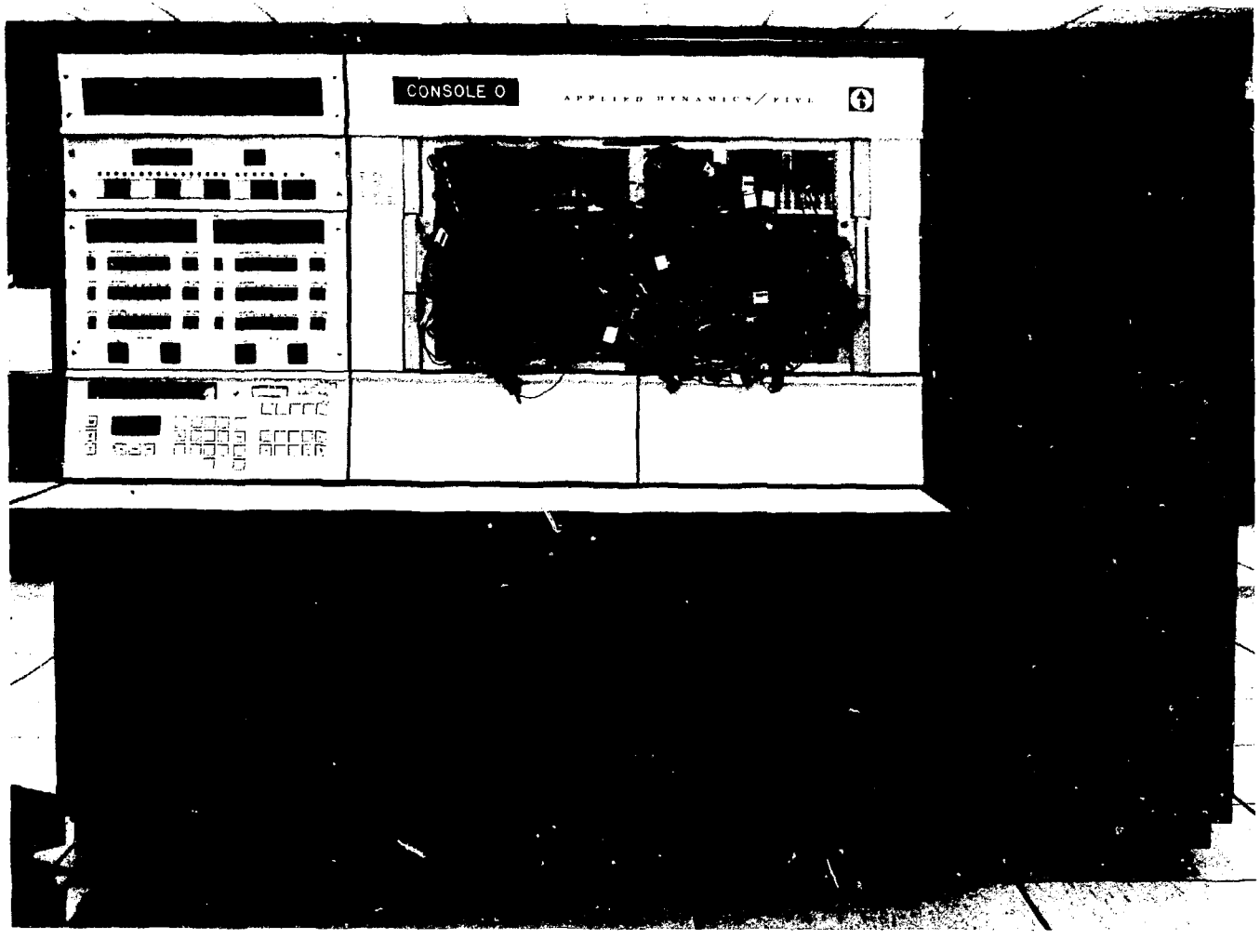

FIGURE 2 ONE OF TWO AD/FIVE ANALOG COMPUTERS

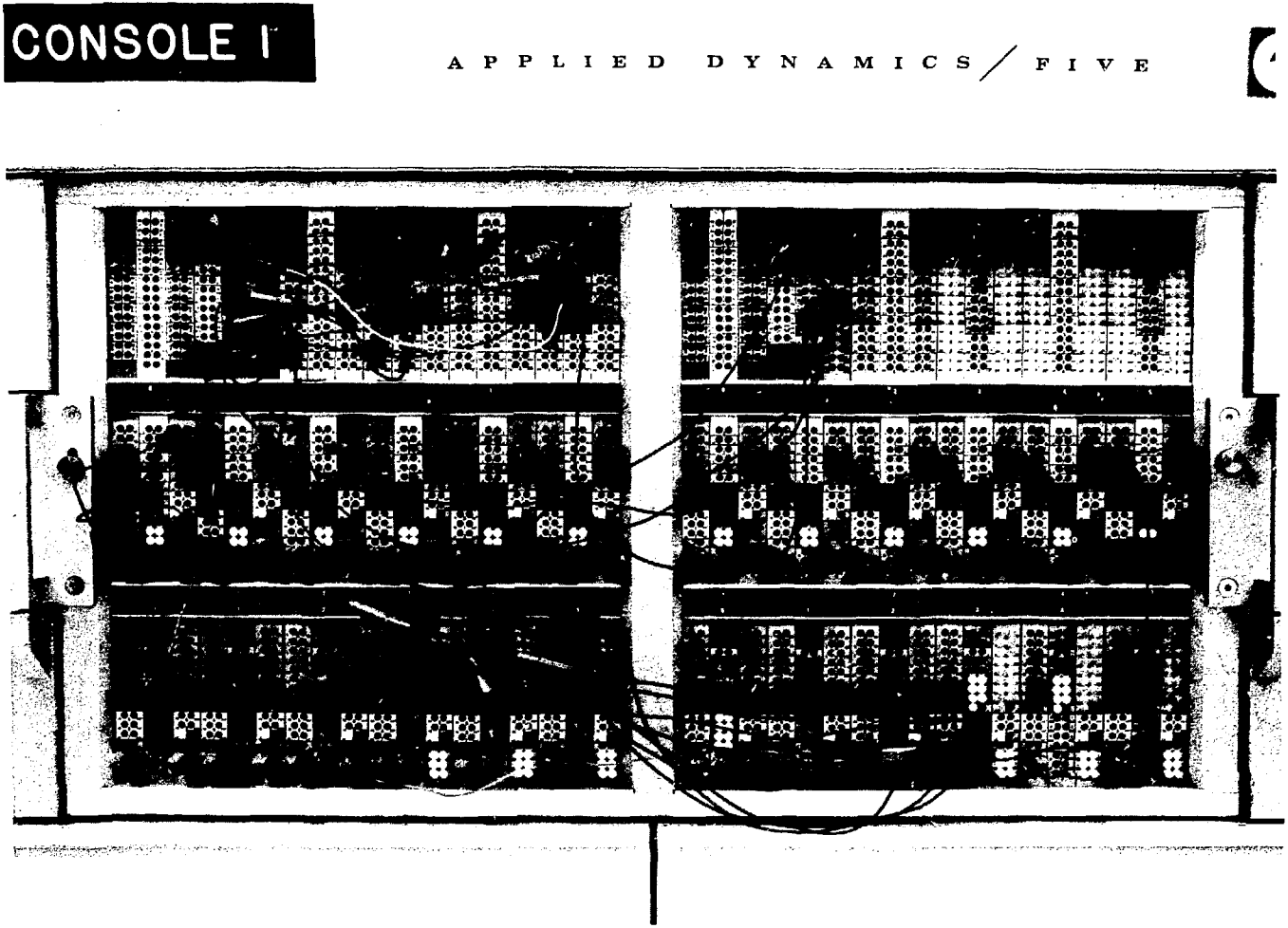

FIGURE 3 AN AD/FIVE PATCHBOARD

2.1.1 Logic Components

One-third of the AD/FIVE patchboard is dedicated to logic computing components. Each console has the following complement of logic components:

16 comparators
8 double-pole-double-throw function relays
48 flip-flops
60 logic gates
8 two-decade binary-coded-decimal counters
6 logic switches
1 interval timer
1 reference timer

As mentioned previously, the logic components are used to control the problem solution. The comparators provide an interface from the analog components to the logic section, while devices such as switch-summers are able to alter analog variables on command from a logic signal. Intergrator modes and time scales may also be controlled (over-ridden) by logic signals. Clocked logic elements utilize a two-phase clocking system to eliminate "race" problems. Many console-control logic signals are also terminated i the logic section of the patchboard. Some of these signals are used for slaving, but in hybrid problems, they are often valuable for synchronizing logic programs with the mode of the analog console.

The reference timer provides a source of fixed period pulses, 1 μs wide. Periods ranging from 1 s to 10 μs, in decade steps, are simultaneously available. Variable period pulses, 1 μs wide, with periods from 10 ms to 1 s, in decade steps, are available when the console is in the X1 time scale. The period of these variable pulses is altered by the console time-scale controls. Thus, if the integrator time-scale is made faster, the logic components, which are using the variable source of pulses, will also run faster by the same factor. This ensures

that the logic program always runs in the same time scale as the analog program.

Many of the logic computing elements have both switches and indicators associated with them. The switches and indicator lamps are located to the left of the patchboard, above the operator control panel. The logic components are not addressable by the AD/FIVE addressing system, but lamps indicate the output logic states. An addressing capability is required in hybrid programs, so a method has been provided to allow the digital computer to read the states of up to 16 logic signals. This is accomplished with a 16-bit digital sense register. Conversely, the digital computer may write up to 16 bits of data to the logic program via the digital control register. Both of these registers are terminated in the logic area of the patchboard.

Access to the nine interrupt lines is also in the logic area of the patchboard. The digital computer is interrupted whenever the logic signal patched to any interrupt line becomes "true".

Devices which have both analog and logic signals, such as comparators and digitally controlled electronic switches, have the logic inputs and outputs terminated in the logic section of the patchboard. Corresponding analog inputs and outputs are terminated in the analog areas.

2.1.2 Analog Components

The lower two-thirds of the patchboard is reserved for analog computing components. Presently, each of the two AD/FIVE computers has the following component complement:

30 integrators (gains of 1, 10, 100, 1000, 10000)
24 summers
30 inverters/summers
24 switch summers
120 digital coefficient units (14 bits + sign)
8 track/store networks
48 digitally-controlled electronic switches
12 hard limiters
8 multipliers (convertible)
4 log generators
2 sine/cosine generators

One integrator solves one first-order differential equation. Therefore, one analog computer of the Dynamic Analysis Facility can solve a set of thirty differential equations in parallel. In the hybrid mode, a set of more than thirty equations may be solved by sharing (multiplexing) the analog hardware. This is done by breaking the equation set into subsets for which there is sufficient hardware and then computing a subset of the solution. The solution subsets are combined to form the complete solution. This method inherently serializes the solution, and the analog computer must run faster than real-time in solving the subsets, to obtain a real-time solution of the set. Usually, the maximum speed of this method is limited by the digital computer.

A distinguishing feature of the Dynamic Analysis Facility is the set of 120 digital coefficient units (DCUs), in place of servo-set potentiometers, in each of the AD/FIVE analog computers. DCUs are single-buffered multiplying digital-to-analog converters, which can be set at high speed, typically 6 μs/DCU by direct memory access. Their four-quadrant operation can replace a potentiometer plus inverter, while their low output impedance results in insignificant loading effects. Settings greater than 1 are permitted, if the output does not exceed

± 10 volts. The maximum setting is ±.6383. They are 15-bit devices (14 bits + sign), with the least significant bit worth 1 millivolt. Data is sent to the DCU control system in twos complement binary format where it is converted to a magnitude and sign, for loading into the DCU register.

The AD/FIVE integrator modes are switched by solid-state field-effect transistor switch circuits rather than relays. The four time scales are obtained by switching both the feedback capacitor and the input resistor, dependent upon which scale is desired. Integrator characteristic times range from 1 s to 0.1 ms. All of the integrators may be configured as 6-input summers, if necessary. Two individual over-riding mode and time scale controls are available for each area of the patchboard.

The value of the output of every addressable computing component can be read via the digital ratiometer (DRM), located in the control panel. This capability makes the DRM invaluable for the set-up and check-out phase of the problem solution; however, its relatively low speed precludes its use in high-speed computation.

A control panel with a complete complement of pushbutton switches is accessible to the operator and affords him complete control of the analog computer. Settings may also be entered into the coefficient devices via this panel. In the hybrid mode, special software routines permit the digital computer to "push the buttons" on the control panel.

2.2 Data Output Devices

One of the features of analog computation is the relative ease with which data may be displayed in graphic form. Since the variables are already represented by voltages, they may be directly applied to any device which records or displays voltage as a function of time, or any other variable. Common devices used are strip-chart recorders, X-Y recorders and cathode-ray oscilloscopes. Each analog console has one of each

of the above instruments. While the oscilloscope and X-Y recorder are mounted in the display rack associated with each analog console (see Figure 4), the strip-chart recorders are free-standing units which may be wheeled to either console.

The two display racks have 10 inter-connecting trunks. Also, 10 of the AD/FIVE analog trunks are brought out to each console's display rack, so easy access to the rack is available from the patchboard.

The two strip-chart recorders have 12 dedicated input lines, while the X-Y recorder and oscilloscope have 2 and 6, respectively. All of these lines are terminated on the patchboard.

2.2.1 Oscilloscopes

Each AD/FIVE analog console has in its associated display rack one Tektronix type R7613, variable-persistence oscilloscope [3]. The oscilloscope mainframe is capable of accepting any Tektronix 7000 series plug-in unit.

The oscilloscope is used for displaying the analog problem solutions and also for debugging both the analog and logic sections of the programs. The variable-persistence feature is ideal for displaying either slow analog solutions or a family of solutions. The mainframes are equipped with the readout option which is convenient for recording oscilloscope settings when photographs are used for permanent records.

Separate amplifiers for the vertical and horizontal axes of the display screen are available in the Dynamic Analysis Laboratory. The plug-in amplifiers for the vertical axis are Tektronix types 7A18 (2 units) [4], 7A22 [5] and 7A26 [6]. The 7A18 and 7A26 units are dual-trace amplifiers which, when used with the R7613 mainframe, give system vertical bandwidths of DC-75 MHz and DC-100 MHz, respectively. These amplifiers have input sensitivities from 5 millivolts/division to 5 volts/division.

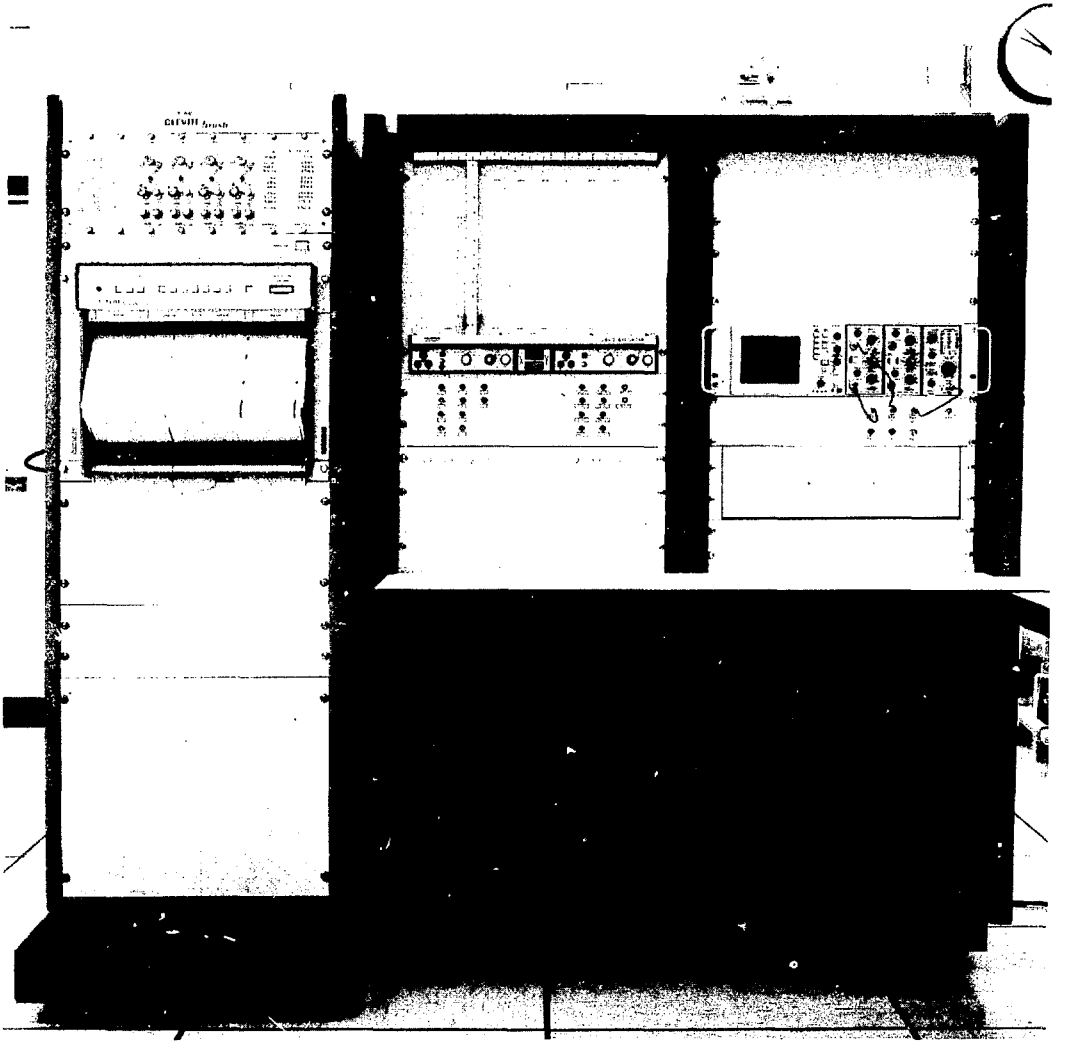

FIGURE 4 ONE OF TWO DISPLAY RACKS

The 7A26 differential amplifier plug-in limits vertical bandwidth of the oscilloscope system to about 1 MHz. This amplifier has high sensitivity, 10 microvolts/division, and switch selectable high-frequency and low-frequency filter cut-off points. It also has the capability of biasing DC offsets. While it is useful as an output device for analog solutions, its main use is as a maintenance and debugging tool.

The plug-in units for the horizontal time base are Tektronix types 7B50 [7] and 7B53N [8]. Both units offer sweep rates from 5 s/division to 50 ns/division. Only the 7B53N unit offers delayed sweep, but both time base units may be used as amplifiers for the horizontal axis, for X-Y type presentations.

Each analog console has the facility for controlling the following oscilloscope functions from the patchboard:

(i) remote erase
(ii) external single-shot reset
(iii) Z-axis, i.e. intensity
(iv) external trigger.

2.2.2 Strip-Chart Recorders

Frequently, it is necessary to examine the relationship of several parameters which vary as functions of time. The easiest way to do this is to simultaneously record all the variables of interest on a multi-channel strip-chart recorder. There are two strip-chart recorders available in the Dynamic Analysis Laboratory, a 4-channel and an 8-channel Gould Brush Series 1707 Mark 200 system [9,10].

Each oscillograph has 12 chart speeds from 0.05 to 200 mm/s. Traces are produced by a pressurized ink system writing on special paper. The system frequency response is flat to 55 Hz full-scale, and to 100 Hz at reduced amplitude.

The 8-channel recorder uses Brush model 13-4215-32 DC preamplifiers [11]. Each amplifier feature calibrated zero suppression and a switchable 5 Hz filter. The input sensitivity

steps are: 1, 2, 5, 10, 20, 50, 100 millivolts/division and OFF. Each of these steps may be used with a X100 attenuation multiplier.

The 4-channel recorder uses Brush model 13-4215-12 high gain DC preamplifiers [12]. Each amplifier has calibrated zero suppression and input sensitivity steps of 0.10, 0.20, 0.50, 1, 2, 5, 10, 20, 50, 100 millivolts/division and OFF. Each of these steps may be used with a X100 attenuation multiplier.

Each recorder has two event-marker pens, one on the extreme right of the chart and the other on the extreme left. These markers may be switched to provide a mark every one second or every ten seconds. An external source may be used to drive the markers when convenient.

The oscillograph or pen-motor and chart-drive system has three possible control modes: partial remote, full remote and local. When the PARTIAL REMOTE button is depressed, chart drive on-off control is transferred to the remote location. Full remote also transfers the chart speed control to the remote location. All control functions are available at the oscillograph front panel when in the local control mode.

The patchboard on each analog computer has the facility for controlling the recorders in partial remote mode and for independently controlling the event markers.

2.2.3 X-Y Recorders

The ability to easily plot one variable as a function of another is a valuable asset in any computation facility. The X-Y recorder is ideally suited to this application. Responses as a function of time may also be obtained on the X-Y recorder by driving the X-axis amplifier with the output from an analog-computer integrator which generates a linear ramp voltage waveform. While most X-Y recorders also offer a built-in time-base for sweeping the X-axis for plots as a function of time, it is often more convenient to use the above method since

it provides inherent synchronization with the other variables, and the X-axis drive is automatically scaled if the analog computer time-scale is altered.

One Houston Instrument Series 2000 Omnigraphic X-Y recorder [13] is mounted in each display rack. Each recorder accepts either standard English 8.5 x 11 inch or 11 x 16.5 inch paper and also standard European A4 (210 x 297 mm) or A3 (297 X 420 mm) paper. Any intermediate or smaller sizes will also work with the vacuum hold down system.

Disposable fibre-tip pens, in black, red or blue are used, and the electric pen lift is actuated either remotely or locally. The pen lift and the X-Y sweep, using the recorder time base, can be controlled from the analog computer patch-board.

3. COMMUNICATION BETWEEN ANALOG AND DIGITAL COMPUTERS

High speed communication between the analog and digital computers, an essential part of a modern hybrid computer, is established via two interfaces [14]. The interfaces are coupled together to form the two-way communications path. Figure 5 shows the location of the interfaces within the Hybrid Computer of the Dynamic Analysis Facility.

The Remote Interface (RIF) is located in the PDP-11/55 digital computer cabinet. The Hybrid Interface (HIF) is located in the analog computer. Electrically, these two interfaces work together as an extension of the digital computer's UNIBUS. There is one unique RIF and HIF for each analog console. Because of this, two independent hybrid programs may be run concurrently on the two analog consoles as long as the PDP-11/55 digital computer is capable of servicing both programs. Multi-conductor cables connect the analog and digital computers via their respective interfaces.

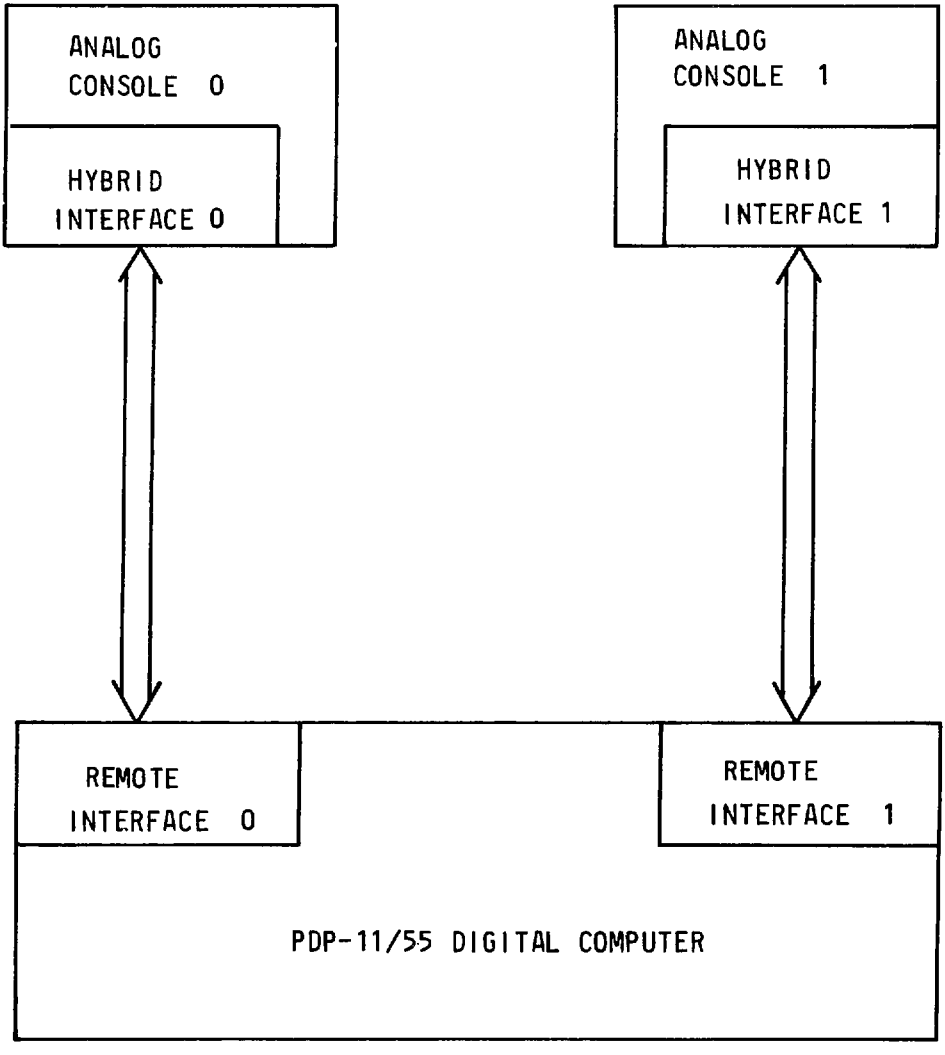

FIGURE 5 BLOCK DIAGRAM OF THE HYBRID COMPUTER

The HIF/RIF communication path is used primarily to

- send "pushbutton" commands from the PDP-11 to the AD/FIVE control system,
- send settings from the PDP-11/55 computer to the coefficient devices,
- read digitized data from the DRM into the PDP-11 memory, and
- read the status of the AD/FIVE, HIF, or RIF.

The transmission of a data or command word by the HIF/RIF system requires less than 2 μs.

While the above satisfies the requirements for a hybrid computer system, another path exists for reading digitized analog variables into the PDP-11/55 computer at very high speed. This is accomplished by the Datawest analog-to-digital converter (see section 3.3 below) which is independent of the HIF/RIF path.

3.1 The Remote Interface

The Remote Interface, located in the PDP-11/55 digital computer cabinet, receives instructions and data from the PDP-11 UNIBUS and data from the analog computer. Depending on the instruction, the RIF performs either an internal function, such as clearing one of its registers, or establishes two-way communication with the analog computer via the hybrid interface.

The RIF also contains the hardware necessary for implementing Direct Memory Access (DMA) communication between the digital and analog computers. The only devices which may receive DMA data from the digital computer memory are the digital-to-analog converters and the digital coefficient units. The Datawest analog-to-digital converter [15] is connected directly to the UNIBUS and therefore does not communicate via the RIF.

Hardware necessary for handling interrupts, generated by the analog computer, is located in the RIF. There are 15 possible interrupts of which 9 are triggered from the patchboard by user programs. The remainder are internally generated to inform communication software of errors or instruction completion.

The RIF can generate only one interrupt vector for the PDP-11 computer. Since there are 15 possible interrupts, an index word is available from a register in the RIF. This word may be examined to determine which interrupt is currently pending. Priority arbitration hardware in the RIF always presents first the pending interrupt with the highest priority.

Interrupt signals are brought directly to the RIF from the analog computer and are not subject to any RIF/HIF communications protocol.

3.2 The Hybrid Interface

The Hybrid Interface is located in the analog computer cabinet. The HIF contains the necessary hardware to access

- the analog computer control system,
- the DAC/DCU system,
- the hybrid interface register and the console status register, and
- digitized analog data from the digital ratiometer.

Data and instructions are routed to all circuit boards in the HIF chassis by a bus which is physically the motherboard of that chassis. Only the circuits that are addressed by the current instruction respond to the signals.

Any hardware that is capable of assuming control of the HIF bus has a bus priority-arbitration circuit to ensure that control of the bus is obtained only when it is not being

used by another device. The priority of these devices is determined by their physical location in the HIF chassis.

While the HIF bus is normally used only for hybrid communications, it is also an integral part of the mechanism for setting DACs and DCUs from the control panel of the analog computer. DACs and DCUs may receive their data from the digital computer in three different ways.

The first is called the slow-speed path. The digital computer sets the device in the same sequential manner an operator would from the control panel of the analog computer. This is done with a software subroutine that "pushes the buttons" in the proper sequence. This takes about 40 ms per device.

A faster method permits the digital computer to directly load the DAC/DCU control system in the HIF with both the command word and the data word. The DAC/DCU control system then loads the data into the addressed device. This takes about 14 μs per device.

The fastest method for setting a group of devices with continuous addresses is Direct Memory Access (DMA), which takes about 6 μs per device, with a startup time of 6 μs.

The ability to treat all of the analog computer's coefficient devices as high speed digital-to-analog converters results in a very powerful facility for hybrid computation. It would not be possible to realize the full benefit of analog computer hardware multiplexing in real time with conventional servo-set potentiometers.

3.3 Analog-to-Digital Converters

The digital computer is able to read the analog voltage, at the output of any addressable analog component, with the digital ratiometer. While this is a very convenient method for the set-up and check-out of a problem, it is not fast enough for high-speed hybrid computation.

The two Datawest analog-to-digital converters [5], located in the digital computer cabinet, are used when fast sampling rates are required. The converters are located in the digital section of the hardware, so they may be interfaced directly to the UNIBUS. This permits the highest possible throughput, since the HIF/RIF path has only one-way DMA transfers from memory to the DACs and DCUs.

Each ADC has 32 channels, all with simultaneous sample/hold capability. The channels are divided into two groups of 16 with a single hold control for each group. The two hold controls are terminated in the logic area of the patchboard. The hold feature is used to eliminate data time-skew that would result from the finite sampling time for each channel.

Each Datawest 301 Series ADC is a semi-parallel device utilizing two eight-bit conversions. The result of the first conversion is entered into an eight-bit, high-accuracy digital-to-analog converter. The second conversion is a digital representation of the difference between the digital-to-analog converter output and the analog voltage input. The results of the two conversions are summed to form a 15 bit (14 bits + sign) word that is accessed by the PDP-11 computer. The least significant bit of the output word corresponds to 1 millivolt of the analog input.

The permissible analog input range is ± 10 volts and the throughput rate is 100 kHz.

3.4 Digital-to-Analog Converters

Each analog console has 16 multiplying digital-to-analog converters, contained in a chassis in the bottom of the analog computer cabinet. These devices are very similar to the digital coefficient units except that they have two buffers, the initial buffer and the final buffer, for storing data (settings). The value at the output of the DAC is always the

product of the input signal and the setting contained in the final buffer. Like DCUs, DACs are four-quadrant devices that receive their data from either the HIF/RIF path or the analog control panel.

DACs have three possible methods for transferring the data in their initial buffer to their final buffer. This data transfer, or updating, can be done in the following ways:

(i) Immediate update: the new setting is immediately entered into the final buffer.

(ii) Digital update: all DACs whose addresses have been stored for digital update are updated when the command is given from the digital computer.

(iii) Patchboard update: all DACs whose addresses have been stored for patchboard update are updated when a logic pulse is applied to the UPDAC hole in the patchboard.

Digital and patchboard update are methods to eliminate time-skew in digital-to-analog converters. All sixteen DACs may be simultaneously updated either by digital or patchboard update.

4. DIGITAL HARDWARE

Presently, there are two digital computers in the Dynamic Analysis Facility. One computer, a DEC PDP-11/45, is the digital processor for the Program Development System, while the other, a DEC PDP-11/55 is the digital processor for the Hybrid Computer.

Initially, when the Hybrid Computer was installed in 1975 March, the digital processor was the PDP-11/45. After two years' experience with this system, it was found that this computer was not fast enough to service the interrupts from the analog consoles for the function generation routines and permit program development to continue when these routines

were running as fast as requested by the users [16]. Therefore, it was decided to separate these two duties, and the PDP-11/55 computer [17] was installed in April 1978 as the digital processor for the Hybrid Computer. The PDP-11/55 computer was chosen for its higher system performance, obtained by the use of high-speed bipolar semiconductor memory, instead of magnetic core memory. Bipolar memory is 2.7 times faster than core memory and thus speeds up instruction execution by a factor of about 2.5. The PDP-11/45 computer then became the digital processor for the Program Development System.

The PDP-11/45 and PDP-11/55 digital computers are powerful tools for high-speed real-time applications and for large multi-user, multi-task applications. As described in the Introduction, a feature required by the analysts of the Dynamic Analysis Section is real-time simulation which implies a high speed of computation. Large simulation models require multiple tasks for controlling the model and analyzing the data from the model. A Program Development System has many users, which implies a multi-task environment.

Therefore, the PDP-11/45 computer was our choice for program development due to its multi-user environment. The PDP-11/55 computer was our choice for dynamic simulation studies because of its high system performance due to the use of high-speed, bipolar, semiconductor memory.

The PDP-11/45 computer (see Figure 6) consists of the mainframe, KW11-L line-clock, M9301-YB multi-device bulk storage bootstrap loader, and FP11-B floating point processor. The storage devices for the system are

- a RK05 disk drive,
- a CDC 9762 disk drive,
- a TU56 DECtape transport, and
- a 9 channel TU10 magnetic tape transport.

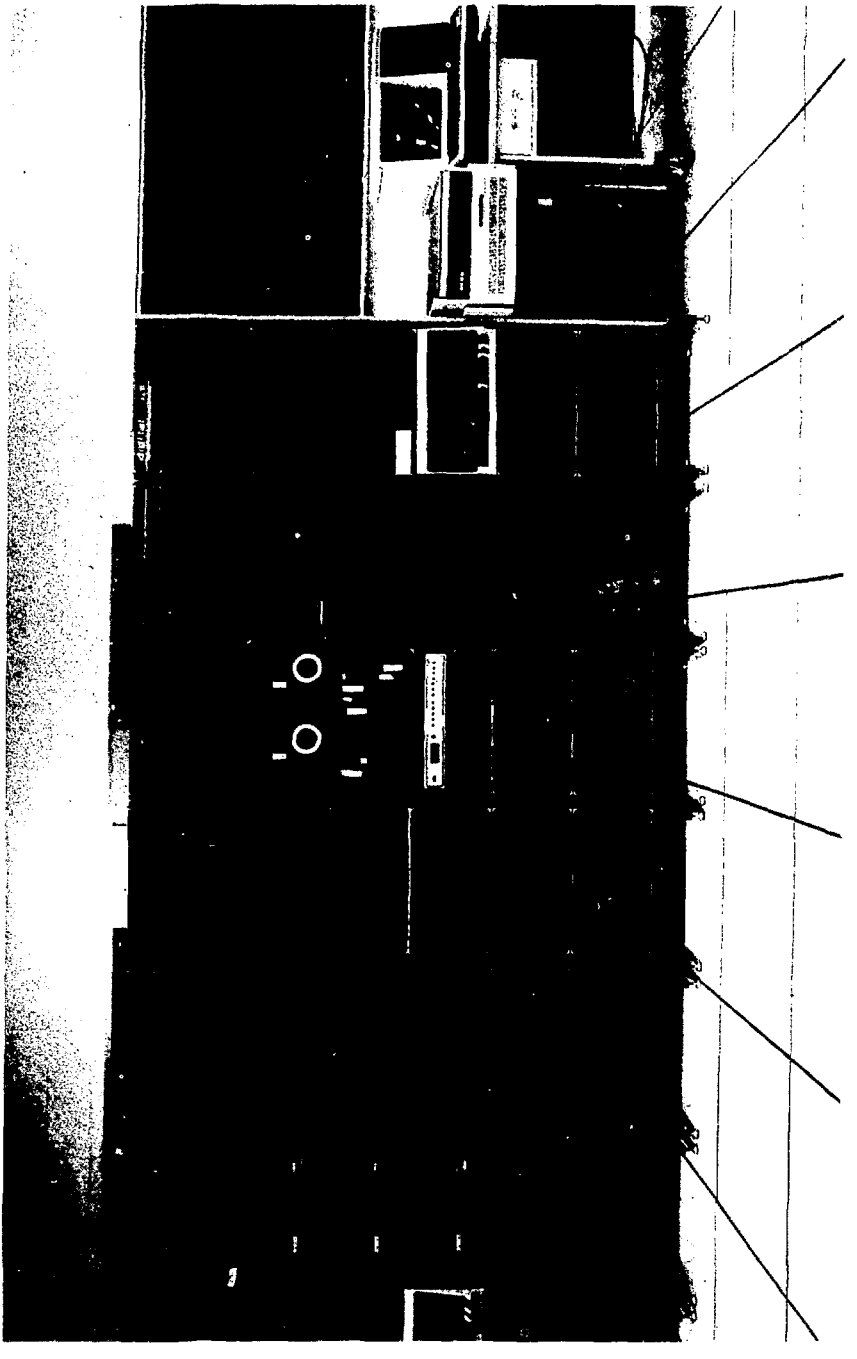

FIGURE 6 THE PDP-11/45 COMPUTER

Users access the computer via any of five terminals,

- a VT05 video display,
- a LA30 DECwriter,
- a VT52 video display, and
- two HP2640A video displays.

The output device for the system is a Versatec 1100A electrostatic printer/plotter which produces listings and plots.

The interprocessor link is a DA11-BD interface.

The PDP-11/55 computer (see Figure 7) consists of the mainframe, KW11-P programmable real-time clock, MR11-DB multi-device bulk-storage bootstrap loader and FP11-C floating point processor.

The storage devices for the PDP-11/55 computer are two RK05 disk drives; the user interfaces are a VT05 video display and a LA30 DECwriter, and the interprocessor link is a DA11-BD interface.

The characteristics of the above hardware units and the interactions between them are described below.

4.1 Central Processors

4.1.1 The PDP-11/45 and PDP-11/55 Mainframes

The central processor unit [17] of either the PDP-11/45 or the PDP-11/55 conputer has a cycle time of 300 ns and contains sixteen general-purpose registers, an arithmetic and logical processor, a memory management unit and a UNIBUS priority-arbitration unit (see Figure 8).

FIGURE 7 THE PDP-11/55 COMPUTER

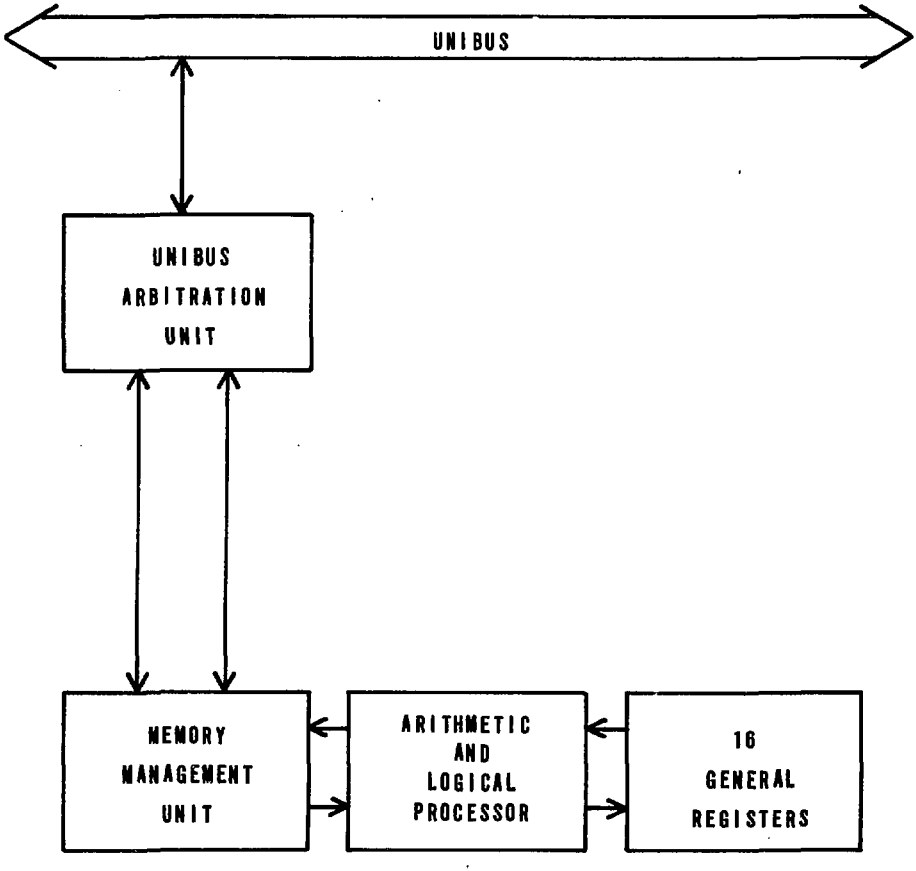

FIGURE 8 DATA PATHS OF THE CENTRAL PROCESSOR

The general purpose registers are used as accumulators, index registers, auto-increment and auto-decrement registers and as stack pointers for temporary storage of data.

Conventional 16-bit computers have

- memory reference instructions,
- operate or accumulator control instructions, and
- I/O instructions.

The PDP-11 computer is different from other mini computers in that all operations are accomplished with one set of instructions. Peripheral device registers can be manipulated as flexibly as core memory by the central processor, and most instructions that operate on CPU registers can also operate on memory or peripheral registers.

The arithmetic and logic processor contains logic for a wide range of operations such as high-speed fixed-point arithmetic with hardware multiply and divide, and extensive test and branch operations.

The memory management unit provides the hardware necessary for complete memory management and protection. It provides the means for assigning memory pages to a user program and preventing that user from inadvertently making any access to pages outside his assigned area. This prevents the user from destroying other programs or the system executive programs.

The user program, i.e. task, may occupy as many as 8 memory pages and each page may be up to 4096 words in length. The relocation feature of the memory management unit allows the base address of each page to be any multiple of 32 words in the 128K (where K=1024) words of physical address space. The memory management unit adds 90 ns to every memory reference when it is enabled.

The UNIBUS priority-arbitration unit regulates UNIBUS requests and transfers control of the UNIBUS to the requesting device with the highest priority.

The PDP-11/45 digital computer contains 124K words of parity core memory, the full complement available, with a cycle time of 980 ns.

The PDP-11/55 digital computer contains 32K words of parity bipolar memory with a cycle time of 300 ns and 64K of MOS semiconductor memory with a cycle time of 475 ns.

System communication is done via the asynchronous UNIBUS. The UNIBUS is a common set of signal wires that connect the processor of one PDP-11 mainframe, its memory and peripherals (see Figure 8). Communication between two devices on the UNIBUS is considered a master-slave relationship in that one device has control of the UNIBUS during any operation. This device, the UNIBUS master, controls the UNIBUS when communicating with another device, called the slave. The maximum transfer rate is one 16-bit word every 400 ns.

4.1.2 Real-Time Clocks

The KW11-L clock [18] in the PDP-11/45 digital computer divides time into 16 2/3 ms intervals. This clock is used by the IAS executive for timing purposes.

The KW11-P clock [18] in the PDP-11/55 digital computer provides programmed real-time interval interrupts and interval counting in 3 modes of operation. Two crystal-controlled signals of 100 kHz and 10 kHz can be used to clock a 16-bit counter. Two external clock inputs (i.e. a 60 Hz line frequency or an external clock input signal) may also be used. The counter may be counted up or down and can be read while in operation. The interrupt sequence is initiated at

zero (underflow) during a count down from a preset interval count. The count-up mode is used to count external events. An interrupt is initiated at zero (overflow).

The programmable real-time clock is used to synchronize real-time events and to detect a time-out of critical computing loops.

4.1.3 Multi-Device Bulk-Storage Bootstrap Loaders

A bootstrap loader is a program that loads another program into computer memory, from a peripheral device, and initiates its execution.

The M9301-YB unit [19] in the PDP-11/45 digital computer has 512 words of read-only memory, containing basic CPU and memory diagnostics, a console emulator program and a specific set of bootstrap programs.

The following storage devices can be booted: RX11 (diskette), TA11 (cassette), TM11 (magnetic tape), TC11 (DECtape), RP11 (RP02/03 disk pack), RK11 (disk cartridge), DL11 (ASR-33 teletype), PC11 (paper tape), RJ03/04 (fixed head disk), RJP04 (disk pack), and TJU16 (magnetic tape). Of the above controllers, only the TM11, TC11, RK11 and the equivalent of the RP11 are available in the Program Development System of the Dynamic Analysis Facility.

When the bootstrap is used, basic CPU and memory diagnostics are run and then the console emulator program is entered. The four console functions, LOAD ADDRESS, EXAMINE, DEPOSIT and START, can be exercised. To initiate a bootstrap loader, a two-letter name of the device to be booted is typed at the terminal, i.e. DK for RK05 disk.

The MR11-DB unit [20] in the PDP-11/55 digital computer is a 64-word bootstrap loader for the following bulk storage devices: RF11 (disk), RK11 (disk), TC11 (dual DECtape), TM11 (9 channel magnetic tape), RP11 (disk), and RC11 (disk).

Of the above controllers listed, only the RK11 is available in the Hybrid Computer of the Dynamic Analysis Facility.

The disk bootstrap is used to load maintenance programs and the IAS executive.

4.1.4 Floating-Point Processors

The floating-point processor (FPP) [21], model FP11-B, in the PDP-11/45 digital computer, performs all floating-point arithmetic operations and converts data between integer and floating-point formats. This processor has

- overlapped operation with the CPU
- high speed

single-precision add and subtract	4.6	µs
multiply	6.6	µs
divide	10.0	µs
double-precision add and subtract	6.2	µs
multiply	12.0	µs
divide	18.4	µs

- single- or double-precision (32 or 64-bit) floating point modes
- same types of addressing as CPU instructions
- six 64-bit floating-point accumulators used in numeric calculations and interaccumulator data transfers
- error recovery aids (i.e. each error causes a trap).

The floating-point processor, model FP11-C [17], in the PDP-11/55 digital computer has the same features as the FP11-B processor above, except that it is faster, i.e.

single-precision add and subtract	1.65	µs
multiply	3.27	µs
divide	4.29	µs

double-precision add and subtract		1.68 μs
	multiply	5.43 μs
	divide	6.73 μs

4.2 Data Storage Devices

4.2.1 Disks

The Program Development Facility has two disk systems, the DIVA model DD-54 and the DEC RK11. The DIVA model consists of a DIVA COMPUTROLLER V controller, a CDC 9762 disk drive and a removable CDC 9877 disk pack. The COMPUTROLLER V controller will control up to 8 CDC 9762 disk drives. The CDC 9877 disk pack has a formatted data capacity of 34.7 million words and the maximum transfer rate is 604K words/s at an average access time of 30 ms. All data transfers to/from the disk utilize a direct memory access (DMA) interface.

The RK11 disk system consists of an RK11 controller, one RK05 DECpack disk drive and one removable disk cartridge. The RK11 controller will control up to 8 RK05 DECpack disk drives. The DECpack disk-cartridge capacity is 1.2 million words, and the maximum transfer rate is 90,250 words/s, with an average access time of 70 ms. All data transfers to/from the disk utilize a direct memory access (DMA) interface.

The two disk systems are utilized in the following manner:

(i) The DIVA disk system acts as 3 DEC RP02 disks, each with a capacity of 10 million words. One RP02 holds the executive, system and maintenance programs, another holds the user and data files and the third is used as a scratch disk.

(ii) System and maintenance programs are supplied on RK05 DECpacks and the RK05 disk drive, labelled C, is used for transferring these programs to the CDC disk pack.

The moving-head disk system [18] in the Hybrid Computer is similar to that described above, i.e. it consists of a RK11 controller, two RK05 DECpack disk drives, and two removable disk cartridges.

Of the two disk drives, A holds a DECpack containing the executive, system and maintenance programs, while B holds a DECpack containing all the user files and data.

4.2.2 DECtape

The DECtape system [18] includes a TC11 dual-transport controller, a TU56 dual transport and two DECtape magnetic tapes. The TC11 controller will control up to four dual transports. The diameter of the DECtape magnetic tape reel is 9.9 cm (3.9 inches), and the reel contains 79 m (260 ft) of tape with a capacity of 147,968 16-bit words. The data transfer rate of the DECtape system is 5K words/s.

The DECtape is used to save files. The user stores data and programs, generated during a session at a terminal, on the disk. When runs are completed, desired data and files can be transferred from the disk to DECtape for backup purposes. All data transfers to/from DECtape utilize a DMA interface.

4.2.3 Magnetic Tape

The 9-channel magnetic tape system [18] consists of a TM11 transport controller, a TU10 tape transport and a magnetic tape. The TM11 controller will control up to 8 transports and is capable of operating with 7- or 9-channel tape transports. The diameter of the magnetic tape reel is 26.7 cm (10.5 in), and the reel contains 732 m (2400 ft) of tape; its capacity is 6 million words, and the data transfer rate is 18,000 words/s. All data transfers to/from tape utilize a DMA interface.

The magnetic tape is used to store programs and large volumes of data. It is the medium used when exchanging data and programs with the CRNL Computing Center and outside companies. The contents of the user disk (the second RP02) are stored on magnetic tape every Monday morning and saved for three subsequent weeks.

4.3 User Interface

Five terminals can be connected to the PDP-11/45 computer and two of them, the LA30 DECwriter and VT05 video display, are provided with switches that allow them to be connected to the PDP-11/55 computer. Furthermore, one of the HP2640A terminals can be switched between the PDP-11/45 computer and the CDC CYBER 170/6600 computer system in the CRNL Computing Center. This is accomplished via a switch, modem and telephone line to the CDC 3300 computer. All of these input-output terminals can be used for

- composing files
- editing files
- forwarding messages to the computer
- receiving instructions and data from the computer
- performing on-line debugging.

4.3.1 LA30 DECwriter

The LA30 DECwriter [18] prints from a set of 64 characters at 300 baud. Data are entered via the 96-character

keyboard, and hard copy is produced on 25 cm (9 7/8 inch) wide paper, the characters being formed by a 5 x 7 dot matrix.

The LA30 terminal will perform the functions listed above, but it is used primarily as a hard-copy device for system generation, software development and initiation of new users.

This terminal is used primarily as the console terminal for both the Hybrid Computer and the Program Development System.

4.3.2 VT52 Video Display

The VT52 video terminal [18] has a display which holds 24 lines of 80 characters of the upper-and lower-case ASCll type. It has a 128 character set, and the characters are formed by a 7 x 7 dot matrix. It is set to transmit or receive at 2400 baud. This terminal can perform any of the functions above, but it is used primarily for the preparation of system and maintenance programs, and also set-up and check-out and control programs for analog models.

4.3.3 HP2640A Interactive Display Terminals

There are two Hewlett-Packard HP2640A interactive display terminals [22]. Each displays 24 lines of 80 characters which are formed by a 7 x 9 dot matrix, and each is set to transmit and receive at 2400 baud, the maximum permissible value. The terminals have four character sets:

- 128-character Roman,
- 96-character Roman (subscript),
- 96-character mathematics, and
- 64-character line-drawing.

Display-enhancement features include blinking, underlining, half-bright and inverse video. Each terminal contains 5K bytes of RAM memory which stores about 3 screens of text.

A HP2640A terminal has block made capabilities. When the terminal is in this mode, typed data are displayed but not transmitted to the computer until requested by the computer or until after the ENTER key has been pressed and the computer has responded. Otherwise, the terminal is in character mode and data are transmitted as typed.

Each of the terminals can perform any of the functions above, but they are used primarily for the preparation of system and maintenance programs and also set-up and check-out and control programs for analog models. As well, they are used for the preparation of Reactor Control Branch engineering files, user's guides, newsletters, etc.

As already mentioned, one of the terminals can be switched to the Computing Centre to permit running of jobs on the CDC CYBER 170/6600 computers from the Dynamic Analysis Laboratory.

4.3.4 VT05 Alphanumeric Video Display

The VT05 terminal [18] consists of a CRT display and a 96-character keyboard. The CRT can display up to 1440 characters at a time, from a 64 character set. The terminal displays 20 lines of 72 characters which are formed by a 5 x 7 dot matrix, and is set to transmit or receive at 2400 baud, the maximum permissible value.

The VT05 terminal can perform any of the functions above, but it is used primarily as an input/output terminal for simulation runs on the Hybrid Computer.

4.4 Data Output Device

The Versatec 1100A printer/plotter [23], part of the Program Development System, consists of a model C-PDP-11 matrix controller and the matrix electrostatic printer/plotter.

As a printer, it prints 132 characters per line at 500 lines per minute. High contrast, 7 x 9 dot matrix characters are printed on 28 cm (11 inch) wide paper. As a plotter, it operates at up to 3 cm (1.2 inches) /s paper speed. with a nib density of 100 dots/inch. Maximum plot width is 26 cm (10.24 inches). The 1100A system also has simultaneous print/plot capability, and a DMA channel is used for data transfer to it when in the plot mode.

The printer/plotter is used mainly as a printer for listing programs as they are edited, assembled and compiled, but it is also used as a plotter to plot data (for example, sampled analog information and Fast Fourier Transforms).

4.5 Interprocessor Links

The DA11-BD [18] interprocessor link provides a means for half-duplex DMA data transfer between the PDP-11/45 digital computer of the Program Development System and the PDP-11/55 digital computer of the Hybrid Computer.

Using the DMA facilities of each computer, the link transfers either single words or blocks of data from the memory of one machine to the memory of the other. The transfer rate can be as high as 500K words/s.

The interprocessor link is used to transfer files between the Program Development System and the Hybrid Computer. These files are usually the set-up and check-out program, control program and data files that were developed on the Program Development System and are required for the setting up and running of an analog model. Output results from the model are sometimes sent to the Program Development System to be plotted or listed on the line printer.

5. SOFTWARE

The IAS operating system, used in both the Hybrid Computer and the Program Development System, is

- disk-based,
- priority-ordered. and
- significant-event driven;

it allows multiprogramming; and it runs in real time.

The IAS operating system in the Program Development System, with utilities and language processors, meets the ease-of-programming criteria for developing detailed system models, mentioned in the Introduction.

In the Hybrid Computer, this operating system, augmented by hybrid software and utilities, meets the criteria of programming ease and good man/machine interaction, mentioned in the Introduction.

Software is required to allow communication between the Program Development System and the Hybrid Computer, and DECNET/IAS fills this role. It offers task-to-task communications, network file transfer and network resource-sharing capabilities.

This section describes the software and how it meets the above criteria.

Documentation of programs and maintenance of hardware are important functions of any computing system. Therefore, documentation aids and maintenance programs are also reviewed.

5.1 IAS Executive

The IAS V3.0 executive [24] is called disk-based because of the following important functions of the disk:

- A back-up copy of the executive is stored on disk to permit system restart.
- All tasks are stored on disk as core images prior to execution.
- Libraries of subroutines used in tasks are stored on disk.
- Files of any kind may be stored on disk and on other mass storage devices.

The executive is defined as priority-ordered and significant-event driven because it performs a scan of the priority-ordered active task list (ATL) when a significant event occurs. By examining the status of the tasks in descending priority order, the executive determines the next task to be initiated or continued. The following cause a significant event

- I/O initialization or queueing of I/O
- normal I/O completion
- request for task execution
- scheduling of a task to be run in the future
- a mark-time directive
- a resume directive
- task completion
- declaration of a significant event.

Multiprogramming of tasks is provided by assigning a software priority level (1-250) to each task. This allows interruption of a lower-priority task when a higher-priority task requires the CPU resources. Event flags are provided to allow the individual task to control its execution and to allow communication with other tasks and the operating system.

The IAS executive is a partitioned system. Partitions are named, contiguous blocks of memory, the number of which is fixed during system generation. All tasks in all

partitions can execute in parallel and partitions are either user- or system-controlled. A user-controlled partition can accommodate only one task at a time, while a system-controlled partition can accommodate as many tasks as can fit into the defined physical space.

The basic program unit, executing under IAS control, is a task consisting of a program module or a set of program modules. Program modules are linked to each other and to the operating system by an overlay task builder and are stored on disk in absolute image form. Task execution can be invoked by other tasks or by a terminal user. Tasks can be specified to execute

- in an indicated memory partition,
- at a given priority,
- under an indicated User Identification Code,
- only if memory is available.

Tasks can be defined as checkpointable, which allows them to be swapped out of memory when space is required for execution of high-priority tasks. Optionally, they can be declared as multi-user tasks which are shareable, allowing more than one user to have access to the pure part of the task, in parallel, by duplicating only the data-dependent code (impure) in memory. The pure part of a task is the part that never changes, but some multi-user tasks have data-dependent code only.

On the Program Development System, the main advantage of the IAS executive is its multi-user capability. We presently utilize four terminals on a full-time basis and can use the VT05 video display as a fifth terminal, as the need arises. These terminals are used mainly for editing, compiling, assembling, task building and running tasks. The tasks produced consist of system programs, utility programs,maintenance programs, set-up and checkout programs and control programs for simulation

runs. All these tasks are stored on the disk. All tasks not related to simulations can be loaded and run when requested, whereas tasks related to simulations are transferred to the Hybrid Computer via the interprocessor link.

The PDP-11/45 digital computer contains 126,976 words of core memory. The layout of this memory is as follows:

Main executive	- 20,960 words
Monitor Control Routine	
Other handlers and file control routines (teletype, DECtape, message output, etc.)	- 23,168 words
TOTAL	= 44,128 words

This leaves 82,848 words available for user and system tasks.

The main advantage of the IAS executive on the Hybrid Computer are the real-time and multiprogramming capabilities. The control of a simulation requires at times many different tasks which are run at different priorities, and therefore the multiprogramming technique is used.

However, for simulation studies, which must run in real time, the IAS executive response to interrupts is not fast enough. The time from the occurrence of the interrupt, until the portion of the device handler [25] that services the interrupt was entered, is 3.3 ms. Therefore, we have modified the hybrid handler to reduce the response time to 125 μs. This is described in Section 5.4 under hybrid software.

The PDP-11/55 digital computer contains 98,304 words of semiconductor memory, one-third of which is bipolar and two-thirds is MOS.

The layout of this memory is as follows:

Main Executive	- 16,480 words
Monitor Control Routine	- 2,048 words
Other handlers and file control routines (teletype, message output, etc.)	- 21,248 words
TOTAL	- 39,776

This leaves 58,528 words available for user and system tasks.

5.2 DECNET/IAS

DECNET/IAS V2.1 software [26] was purchased to allow communication between the Program Development System and the Hybrid Computer. This software allows

- device sharing, i.e. access to the peripheral devices of a remotely located system,
- file sharing, i.e. access to files stored on a remote system,
- program sharing, i.e. the running of a program on the remote system, and
- inter-task communication, i.e. creation of a data path for transfer of information between two tasks in the same system or in remotely located systems.

Presently we are using only two of the above functions, i.e. device sharing and program sharing. Users of the Hybrid Computer access the disk and the line printer on the Program Development System. Thus, all control programs for hybrid simulations are developed on the Program Development System and transferred to the Hybrid Computer for execution via the interprocessor link. All the functions of the DECNET software will be utilized when large simulations are developed and when process hardware, such as control computers, is added to the system.

The DECNET software must be in memory only when required. It can be loaded or removed at any time, but when first loaded, an initialization process takes place, requiring 14,912 words of memory. After the initialization has been completed DECNET occupies 17,888 words of memory.

5.3 Language Processors

Many languages are available to the user of the Dynamic Analysis Facility, and the language he chooses depends greatly on the problem at first hand and how he wishes to solve it. The processors available are FORTRAN-IV PLUS (F4P), RATFOR (RAT), MACRO-11 assembler (MAC), BASIC and the Interactive Hybrid Interpreter (IHI). These processors and their attributes are discussed below.

FORTRAN IV-PLUS (F4P) software [27] is a complete implementation of FORTRAN based on American National Standard (ANSI) FORTRAN-66, with numerous extensions. The FORTRAN IV-PLUS compiler produces PDP-11 machine code optimized for execution time on a PDP-11 computer with a floating-point processor.

Timing tests were performed on tasks compiled with the manufacturer's standard FOR compiler, and similar ones compiled with F4P. Tasks compiled with F4P ran 50-60% faster, and the task images were of the same size or smaller.

Since the F4P compiler produces machine code, it is easy to debug a FORTRAN program because the octal debugging technique (ODT) program may be used. This feature is not available with FOR. Users tend to program mostly in FORTRAN as it is a universal higher-level language and is easier to use than assembler language. Programming in assembler language would increase the speed of a program by only 10% at most, and this could be achieved only by a very proficient programmer. The assembler language is also much more difficult to learn than FORTRAN.

The RATFOR processor [28] is a FORTRAN preprocessor which supports a number of language extensions not found in FORTRAN. It allows use of structured programming techniques in a FORTRAN program, thereby generating an easy-to-understand program. The RATFOR processor translates programs written in the RATFOR language into FORTRAN. This output is then presented to the FORTRAN compiler for processing.

If the user desires to write a program that will execute in the shortest time possible, then he programs in the MACRO assembler [29] language. This language has an instruction complement which uses the flexibility of the general-purpose registers to provide over 400 powerful instructions.

If the user wishes to interact with his program and is not concerned about speed of execution, then he can use the BASIC [30] and IHI [31] languages. BASIC and IHI are conversational high-level programming languages which use straightforward English-like statements and familiar mathematical notation to perform operations. Compared to BASIC, IHI has an advantage in its hybrid capabilities, described in section 5.4.

All of these processors are used in the Program Development System. The user assembles, compiles and then task-builds his program on the system. If the task is to be run on the Hybrid Computer, it is then transferred via the interprocessor link. All these processors, except BASIC, may be utilized in the Hybrid Computer if required.

5.4 Hybrid Software

The hybrid software in the Hybrid Computer consists of a hybrid handler, hybrid communication routines and an Interactive Hybrid Interpreter.

Under IAS, the AD/FIVE device handler is the software interface between the analog and digital computers. As one of its functions, the handler must service interrupts generated by the analog computer. Because of the continuous nature of analog computing, it is important that these interrupts be acted upon as soon as possible.

The handler supplied with the system was found to be too slow in servicing interrupts (3.3 ms) and hence was modified to improve this response time to 125 μs. This modification included writing some Fast Interrupt-Service (FIS) routines [32]. When an interrupt occurs from the analog console, control is passed to one of the FIS routines. These routines are initialized by the user through a FORTRAN CALL statement, to pass the parameters and prepare for interrupts. Capabilities provided are

- transport delays
- function generation
- function storage and playback
- high speed analog-to-digital conversion with buffering
- output of a stored function to an oscilloscope or plotter.

The Hybrid Communication Routines (HCRs) [33] provide all the basic AD/FIVE control-panel operations. These routines are written in assembler language, and they communicate with the analog consoles through the hybrid handler. The HCRs can be accessed from FORTRAN, MACRO and the Interactive Hybrid Interpreter (IHI), and are used to set up and control the analog console(s).

The Interactive Hybrid Interpreter (IHI) [31] is an interactive, easy-to-use, interpretive programming language. Interactive hybrid communication capability is essential for efficient analog and hybrid program development and debugging. IHI is useful in a hybrid system in much the same way that "on-line-debugging" features are often indispensable in digital

program debugging. IHI has all the necessary statements (via subroutine calls) to "push the buttons" on the analog computer, as well as the basic hybrid communication capability provided by the HCRs. IHI also allows direct access to the components in the analog computer by means of convenient analog device mnemonics.

5.5 Utility Programs

Many utility programs have been purchased or written by our personnel since the arrival of the system. These, and some of the utility programs provided with the system, are listed below.

The following utilities are available on both the Hybrid Computer and the Program Development System.

(i) The Peripheral Interchange Program (PIP) [34] is an IAS file utility program that transfers data files from one standard FILES-11 device to another, i.e. PIP can

- copy files from one device to another,
- delete files,
- rename files,
- list file directories,
- set the default devices and UIC for PIP operations,
- unlock files, and
- spool files for printing.

(ii) The Line Text Editor (EDI) [34] is a line-oriented editor that allows for the creation and modification of text files.

(iii) The Set-up and Check-out Utility (SCU) [35] program takes the user's data and patching description and sets up and checks the analog computer.

(iv) The MCR Indirect File Processor [36] is used for interpreting commands from a file. This processor reads the command file and interprets

each command line either as a command to be passed to the MCR or as a request for action by the processor itself.

(v) A FORTRAN IV-PLUS OTS [37] shareable library was built and is available to the users.

(vi) The Task Builder (TKB) [38] links the user's object modules, resolves any references to shareable global areas and produces a single task image which is ready for installation and execution.

(vii) The TECO editor [39] is a character-oriented editor.

(viii) The Librarian Utility Program (LBR) [34] allows for the creation, updating, modification, listing and maintenance of object and MACRO library files. A library file is a direct-access file containing one or more modules of the same module type. Library files are organized for rapid access by the Task Builder and MACRO-11 assembler.

(ix) The Device Unserviceable Documentor (DUD) [40] is a program that allows the users to log hardware and software complaints and to recall complaints that have been encountered by others but have not yet been resolved.

(x) MCR Command Utilities [41] are a group of command files that provide a generalized compile, task-build and run capability. These command files are processed by the MCR Indirect File Processor.

The following utilities are available on the Program Development System only.

(i) The File Transfer Program (FLX) [34] is a file utility program that performs file conversion between DOS-11 or RT-11 and FILES-11 format.

(ii) The Scientific Subroutine Package [42] is a collection of more than 100 FORTRAN subroutines which provide the user with a large cross-section of commonly used mathematical and statistical routines.

(iii) The GRAPHIC package [43] is a set of subroutines that simplify the use of the Versatec printer/plotter for plotting results.

(iv) The NDCU routine [44] is used to convert a patchboard hole number into a hybrid address.

(v) MTRW [45] is a subroutine for convenient use of magnetic tape from FORTRAN.

(vi) FFTSC [46] is a subroutine that performs a radix-2 fast Fourier transform. A forward or inverse transform as well as a power spectrum may be calculated.

(vii) HPXFR [47] is a program used to transfer data between the HP9820A calculator and the PDP-11/45 digital computer.

(viii) The Dynamic Analysis Facility Versaplot Package [48] is the original Versaplot II version 06 package with enhancements to make it more convenient to the user. The Versaplot Package utilizes a two-phase plotting technique. In the first phase, the entire plot image is generated in vector data. The vector data are converted, in the second phase, to raster form for plotting.

5.6 Documentation Aids

One of the major responsibilities of any programmer is the documentation of his work. To aid the user in this task, the following programs have been purchased or written by the system personnel and are available on the Program Development System.

(i) RUNOFF [49] is a program to facilitate the preparation of typed or printed manuscripts.

(ii) The Hewlett-Packard Editor (HPE) [50] is a program that operates with the IAS executive to support the block-mode editing capability of the Hewlett-Packard model 2640A terminal.

(iii) The Hewlett-Packard printer (HPP) [50] is a program used with the IAS executive to print the character code generated by a Hewlett-Packard terminal model 2640A.

(iv) LST [51] is used to format listings for documentation. It provides a standard header and adequate margins on all sides.

(v) EXTRAC [51] is an MCR command file that extracts a brief user's guide from the comments of a source program.

5.7 Maintenance Programs

Digital Equipment Corporation (DEC) supplies maintenance programs to test individual components and peripherals of the PDP-11 digital processors. Also supplied by DEC is a system exerciser program that exercises all the components and peripherals of the PDP-11 system. This exerciser is run on both digital computers during non-working hours. By leaving the processor power on and using this exerciser, the number of failures of the digital processor and peripherals has greatly decreased.

The communication paths between the digital and analog computers on the Hybrid Computer are checked by the following maintenance programs.

(i) The Linkage Diagnostic Program (LKD) [52] enables the user to check the hardware operation of the AD/FIVE computer and the HIF/RIF interface.

(ii) The COEF program [53] checks the DMA and NON-DMA path for DACs and DCUs on the AD/FIVE computer.

(iii) The INTEST program [54] checks all operations of the integrators on the AD/FIVE computer.

(iv) The ADC program [55] checks most aspects of the Datawest ADC operation.

(v) The HYCOM program [56] checks the AD/FIVE hybrid-communication data lines.

6. SYSTEM UTILIZATION AND RELIABILITY

On average, there are nine people using the system on essentially a full-time basis. Five of them are developing and running simulations and four are maintaining and developing system hardware and software. Between them, they use the four terminals on the Program Development System 90-95% of the time. The analog consoles on the Hybrid Computer are used about 30% of the time. The reason for this difference in utilization is that preparation of digital programs and patching of the analog boards requires much more time than actual production runs on the analog computers.

The system has been reliable. Over the past 4 years, the PDP-11/45 digital system was down for 1-2 weeks, mainly because of problems with the disks and magnetic tape. The PDP-11/55 computer had several early bipolar memory failures but has since been very reliable.

The analog computers were also down for 1-2 weeks and require, on a continuing basis, about one man-day a month for repair and calibration. Many of the initial problems were traced to a bad batch of operational amplifiers and to poorly soldered joints. This is to be expected for a new piece of hardware, especially one that contains several design innovations.

From an overall viewpoint, the Dynamic Analysis Facility has met our expectations, as a powerful computing system, in all respects and exceeded them in others. For example, the foreground/background operating software envisaged earlier [1], has been acquired in the form of a general, multi-user, priority-ordered system that provides considerably more flexibility in the utilization of the Facility.

As expected, the software supplied by the manufacturers of the various components of the Dynamic Analysis Facility (digital, analog, peripherals), while acceptable for general-purpose hybrid computation, had to be considerably revised and extended to meet our special needs.

In common with the owners and operators of other computing systems, we find that our Facility is in a state of continuous change. The software is being improved and expanded, while hardware modifications and additions are in progress, to make the Facility even more efficient and to increase its capability. A major advance in this regard will be realized when the Dynamic Analysis Facility becomes part of the computer network currently being implemented at the Chalk River Nuclear Laboratories.

7. ACKNOWLEDGMENTS

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